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10/594,827	09/28/2006	Pedro Chaparro Monferrer	P23882	8377

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	PAPER NUMBER
2115	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,827	MONFERRER ET AL.	
	Examiner	Art Unit	
	VINCENT T. TRAN	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-23,25-43 and 45-51* is/are rejected.

7)☒ Claim(s) *24, 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 8/17/2009.

2. Claims 21-51 are pending for examination.

Claim Objections

3. Claim 23 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 21, 23, 25-27, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson in view of Acar et al. US Pub. No. 20050044515 ("Acar").

5. As per claim 21, Jacobson teaches an apparatus comprising:

a first logic circuitry [106 fig. 7] to generate a first signal corresponding to one or more sensed temperature values [*paragraph 0099 – the apparatus use a plurality of sensor, first, second, and third sensors 106, 106', and 106"; the sensor 106 can be a voltage sensor, a current sensor, a temperature sensor*]; and

a second logic circuitry [106' see fig. 7] to generate a second signal corresponding to one or more voltage values; and

a third logic [104] to generate a third signal [*paragraph 0092 –The controller receives data from the sensor and dynamically modify operation of the controllable semiconductor 102 via the control signal*] corresponding to a leakage power value based on the first signal and the second signal [paragraph 0148-0149].

Although Jacobson teaches the operating parameters of the controllable semiconductor that can be measured included drain voltage, gate voltage....temperature. Jacobson does not expressly teach the one or more voltage values are to comprises a current value of a threshold voltage and a current value of a supply voltage.

Acar teaches another invention relates to methods for determining full chip leakage to optimized the design of an IC. Specifically, Acar teaches leakage power is strongly affected by environmental variables (power supply voltage, temperature) and process variations (effective channel length, threshold voltage, etc.) [paragraph 0032].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Jacobson with the sensing of one or more current value of a threshold voltage and current value of a supply voltage in order to obtain an accurate leakage value since, as taught by Acar, the leakage power is strongly affected by the threshold voltage and supply voltage.

6. As per claim 23, see discussion in claim 1.

7. As per claim 25, Jacobson teaches the leakage power value corresponds to leakage power consumed by a device to which the sensed temperature values and the one or more voltage values correspond [paragraph 0148].

8. As per claim 26-27, Jacobson teach a storage unit [fig 8 – nonvolatile memory, A/D and D/A converters] to store a plurality of temperature value or voltage values, wherein the first and second logic generates the first signal and second signal based on one or the plurality of stored temperature, voltage values [inherent].

9. As per claim 29, Jacobson teaches one or more temperature sensors to sense the temperature value [106 fig. 8].

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson/Acar as applied to claim 21 above, and further in view of Lovett US Pub. No. 20050125597.

11. As per claim 22, Although Jacobson teaches, during the operation of the device, the controller receives data from the multiple sensors, so that the controller can dynamically modify operation of the device via the control signal to prevent over-current, over voltage, excessive

power. However, Jacobson does expressly teach a fourth logic to adjust power consumption of one or more components of a computer system based on the third signal.

Lovett teaches another invention relates to a IC device, and, more specifically, to providing a oscillator scheme that is capable of compensating for external factors, such as voltage, temperature, and process. Specifically, Lovett teaches adjusting the device power consumption based upon an estimation of power leakage at a given range of temperature, operation voltage [paragraph 0031-0032] wherein the device comprising a fourth logic [310 fig. 3] to adjust power consumption of one or more component [240 fig. 2] of a computer system bases on the third signal [325 fig. 3].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Jacobson/Acar with a fourth logic to adjust power consumption in order to reduce standby current and save power as taught by Lovett [paragraph 0008, 0032].

12. Claims 28, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson/Acar as applied to claim 21 above, and further in view of Huard et al. US Pub. No. 20030206050 ("Huard').

13. As per claim 28, Jacobson teaches the calculation of power leakage using the expression discloses in paragraph 0148 and 0149. Jacobson does not teach a storage unit to store a plurality of leakage power values, wherein the plurality of leakage power values are indexed by temperature and the voltage.

Huard teaches another invention relates to controlling the operating conditions of a clock generator as a function of the operating temperature and instantaneous voltage of the circuit. Specifically, Huard teaches a storage unit [paragraph 0028 - tables stored in read only memory] to store plurality of frequency values [F], wherein the plurality of frequency values are indexed by the temperature [T] and the voltage [Vnow] [paragraph 0024, 0028].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Jacobson/Acar with the storage unit of Huard to store a plurality of leakage power values, wherein the plurality of leakage power values are indexed by the temperature and the voltage since this technique is well know in the art of pre-test system parameter. The motivation for doing so would have been to reduce processing power which would reduce power consumption and processor's utilization.

14. As per claim 30, Huard teaches the frequency responder 66 is coupled to receive the outputs Vnow and T of the voltage sensor and the temperature sensor and, in response to them, provides a control signal F to the clock generator to control the clock. Therefore, Huard teaches a multiplier equivalent circuit to multiply to first [T] and second signals [Vnow] to provide the third signal.

15. As per claim 31, Huard teaches a processor cores [paragraph 0022 – where the load circuit 16 can be a microprocessor], the first logic [62], the second logic [64], or the third logic [66]. Huard does not teaches the processor core comprising the first logic [62], the second logic [64], or the third logic [66]. However, such feature is well know in the art of circuit design. One of routineer in the art would wanted to include first logic [62], the second logic [64], or the third logic for portability.

16. As per claim 32, Huard teaches a processor cores [paragraph 0022 – where the load circuit 16 can be a microprocessor], wherein at least one of the one or more processor cores, the first logic [62], the second logic [64], and the third logic [66] are on the same die [60]

17. Claims 33-39, 41-43, 45-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson in view of Huard and Acar.

18. As per claim 39, Jacobson teaches a method comprising:

determining a temperature scaling value [fig. 8 – the controller comprising a nonvolatile memory, A/D and D/A converters] corresponding to one or more temperature values sensed from a device [106 fig. 7];

determining a voltage scaling valued based on one or more voltage values corresponding to the device [106' fig. 7] ; and

calculating a reference leakage power value of the device based on the temperature value and the voltage value [paragraph 0148-0149] to generate a signal corresponding to a leakage power of the device [*paragraph 0092 –The controller receives data from the sensor and dynamically modify operation of the controllable semiconductor 102 via the control signal*].

Jacobson does not teach scaling a reference leakage power value and one or more voltage values are to comprises a current value of a threshold voltage and a current value of a supply voltage.

Acar teaches an invention relates to methods for determining full chip leakage to optimized the design of an IC. Specifically, Acar teaches leakage power is strongly affected by

environmental variables (power supply voltage, temperature) and process variations (effective channel length, threshold voltage, etc.) [paragraph 0032].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Jacobson with the sensing of one or more current value of a threshold voltage and current value of a supply voltage in order to compute an accurate leakage value since, as taught by Acar, the leakage power is strongly affected by the threshold voltage and supply voltage.

With regard to the limitation scaling a reference leakage value based on the temperature and voltage scaling value, Jacobson teaches the controller solves the non-linear equations as show in paragraph 0148 to obtain the leakage value based on the temperature and voltage scaling value. In other words, Jacobson does not teach table to store a plurality of reference leakage values, wherein the plurality of leakage power values are indexed by the temperature and the voltage. However, such feature is well know in the art where device is common pre-tested to obtain the reference values such that the device does not required to compute for reference values during runtime.

Huard teaches another invention relates to controlling the operating conditions of a clock generator as a function of the operating temperature and instantaneous voltage of the circuit. Specifically, Huard teaches determining a temperature/voltage scaling value based on one or more temperature/voltage values sensed/corresponding to the device [*paragraph 0024, 0028 – the voltage and temperature sensor can include A/D converter, which output multi-bi binary signals Vnow and T*], and scaling a reference frequency value [F] of the device based on the

temperature scaling value and the voltage scaling value [*response to Vnow and T, the responder 66 provides a control signal F*].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Jacobson with the method taught by Huard to store a plurality of reference leakage power values, wherein the plurality of leakage power values are indexed by the temperature scaling value and the voltage scaling value. The motivation for doing so would have been to reduce processor usage which would reduce power consumption.

Therefore, it would have been obvious to combine Jacobson with Acar and Huard to obtain the invention as specified in claim 33.

19. As per claim 34, Jacobson [paragraph abs] and Huard [paragraph 0024, 0028]teach sensing and scaling are performed during run-time of the device.

20. As per claim 35-36, inherent since Huard teach a converter to convert sensed temperature/voltage to a binary signal.

21. As per claim 37, see discussion in claim 30.

22. As per claim 38, Huard inherently teach the scaling the reference F values are determined during test or design of the devices. Therefore, the system of modified by Huard teaches the limitation of claim 38.

23. As per claim 39, Jacobson teaches a computer system comprising:

a memory [fig. 8 – nonvolatile memory] to store a plurality of bits representing a plurality of scaling factors;

a first logic [LOAD 150] having one or more components to perform one or more computing operations; and

a second logic [controller 104] to compute the leakage power values corresponding to at least one of the one or more components based, at least in part, on sensed temperature variations [temperature 106] and one or more of the plurality of stored scaling factors.

Jacobson does not teach scale a base leakage power value and stored scaling factors corresponds to a current value of a threshold voltage and a current value of a supply voltage.

Acar teaches one or more voltage values are to comprises a current value of a threshold voltage and a current value of a supply voltage [see discussion in claim 33 – therefore it would have been obvious to one of routineer in the art to stored scaling factors corresponds to a current value of a threshold voltage and a current value of a supply voltage] and Huard teaches scaling a base leakage power value [see discussion in claim 33].

24. As per claim 41, Jacobson inherently teaches at least one or the plurality of stored scaling factors corresponds to a voltage scaling value [since Jacobson teaches nonvolatile memory and A/D converter to convert sensed voltage]

25. As per claim 42, Jacobson teaches the voltage scaling value corresponds to one or more voltage values [a/d conversion].

26. As per claim 43, see discussion in claim 21.

27. As per claim 45, Jacobson inherently teaches the plurality of stored scaling factors comprising a plurality of temperature scaling values and a plurality of voltage scaling values [see fig. 8].

28. As per claim 46, Jacobson teaches the memory comprises a read-only memory [inherent since Jacobson teaches memory stored manufacture's data sheet – paragraph 0097].

29. As per claim 47-48, see discussion in claim 31-32.

30. As per claim 49, Huard teaches the one or more computing operating comprise one or more of data processing [processor].

31. As per claim 50, Huard does not teach an audio device. However, such device is well know in the art.

32. As per claim 51, Jacobson teaches one or more sensors to sense the temperature variation [fig. 7].

33. Claims 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson/Acar/Huard as applied to claim 39 above, and further in view of Lovett.

34. As per claim 40, Although Jacobson teaches, during the operation of the device, the controller receives data from the multiple sensors, so that the controller can dynamically modify operation of the device via the control signal to prevent over-current, over voltage, excessive power. However, Jacobson does expressly teach a fourth logic to adjust power consumption of one or more components of a computer system based on the third signal.

Lovett teaches another invention relates to a IC device, and, more specifically, to providing a oscillator scheme that is capable of compensating for external factors, such as voltage, temperature, and process. Specifically, Lovett teaches adjusting the device power consumption based upon an estimation of power leakage at a given range of temperature, operation voltage [paragraph 0031-0032] wherein the device comprising a fourth logic [310 fig.

3] to adjust power consumption of one or more component [240 fig. 2] of a computer system bases on the third signal [325 fig. 3].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Jacobson/Acar with a fourth logic to adjust power consumption in order to reduce standby current and save power as taught by Lovett [paragraph 0008, 0032].

Allowable Subject Matter

35. Claims 24, 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINCENT T. TRAN whose telephone number is (571)272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vincent T Tran/
Examiner, Art Unit 2115